Remarks

Applicants noticed that the cancellation of claim 2 in the previously filed amendment has not been acknowledged by the latest Office action. Applicants respectfully request the entering of said amendment.

In the non-final Office action, claims 1-8 are rejected under 35 USC § 103(a) as being unpatentable over Manley et al. (U.S. Patent No. 5,108,939) in view of Chang (U.S. Patent No. 6,160,287). The rejection is respectfully traversed.

In the Office action, the Examiner states, "Manley et al. fail to disclose a main gate region and a small sidewall spacer electrically coupled together by a connecting layer, wherein the connecting layer being formed over and in contact with both the small sidewall spacer and the main gate region. Chang discloses a main gate region 60 and a small sidewall spacer 76 electrically coupled together by a connecting layer 80, wherein the connecting layer being formed over and in contact with both the small sidewall spacer and the main gate region."

Applicants respectfully submit that Manley et al. fail to teach or suggest Applicants' claimed invention and the missing teachings are not supplemented by Chang. Specifically, the spacer 239 of the present invention is connected to the **floating gate** region 212, not to the **main gate** region, as it is stated in the Office action. As is clearly stated in claim 1 of the present invention, the floating gate includes "a main **floating gate** region and a small sidewall spacer electrically coupled together by a connecting layer, said connecting layer being formed over and **in contact with both said small sidewall spacer and said main floating gate region.**" In contrast, the spacer in Chang is not connected to the floating gate by a connecting layer. In fact, the spacer is not even connected to any part of the main

gate. According to specification in Chang, the metal silicide layer 80 is defined as the select gate layer in the flash memory. (column 4, line 67 - column 5, line 1) Assuming that the statement is accurate, then, the silicide layer 80 is part of the select gate and could not have been in contact with either the control gate or the floating gate of the main gate region. Figure 12 is quite misleading in that it depicts the silicide layer 80 connecting the spacer 76 to both the control gate 60 and the floating gate 62. Applicants do not understand how the flash memory cell could function if the control gate 60 is shorted to the floating gate 62 by a metal silicide layer 80. One can only postulate that there exist an insulation layer between the silicide layer 80 and the main gate region 60 and 62. Provided that the silicide layer 80 is part of the select gate, then, the Chang patent could not have disclosed "a main gate region of 60 and a small sidewall spacer 76 electrically coupled together by a connecting layer 80," as stated in the Office action.

The connection between the main floating gate region and the spacer by the overhanging connecting layer is a distinctive feature of the invention. As stated in the Summary of the Invention, "both the small sidewall spacer and the main floating gate region are formed on a substrate and both form the floating gate of the non-volatile memory cell. Both are isolated electrically from the substrate by an oxide layer that is thinner between the small sidewall spacer and the substrate; and is thicker between the main floating gate region and the substrate. The small sidewall spacer can be made narrow; therefore, the thin portion of the oxide layer can also be made small to create a small pathway for electrons to tunnel into the floating gate." As is well known to one skilled in the art, the tunnel oxide, whereupon the spacer sits, should be as thin as possible so that a lower voltage is required to induce the Fowler-Nordheim tunneling effect. As shown in Figure 3, the spacer 239 of the present invention

sits on a much thicker oxide layer 208. Contrary to the teaching of the present invention, Figure 12 of the Chang patent shows a spacer 76 sitting on an oxide layer that is thicker than the oxide on which the floating gate 62 sits. In the figure, the floating gate 62 sits on oxide layer 52 while the spacer 76 sits on top of a thicker oxide region composed of the oxide layer 52 and an additional oxide layer 70. So, in fact, far from rendering the present invention obvious, the Chang patent actually teaches away from the present invention.

Conclusion

In view of the remarks made herein, Applicants request reconsideration of claims 1, 3-8. A Notice of Allowance is earnestly solicited.

CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313

Signed: Sally Azevedo
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Date: August 22, 2003

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